UNITED STATES PATENT APPLICATION

OF

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FOR

METHOD OF FABRICATING A LIQUID CRYSTAL DISPLAY PANEL

[0001] The present invention claims benefit of Korean Patent Application No. P2000-87049 in Korea on December 30, 2000, which is hereby incorporated by reference.

BACKGROUND OF THE INVENTION

FIELD OF THE INVENTION

[0002] This invention relates to a flat panel display device, and more particularly to a method of fabricating a liquid crystal display panel suitable for providing a picture of high brightness.

DESCRIPTION OF THE RELATED ART

[0003] In general, there are several flat panel display devices including liquid crystal display panels, electro-luminescence panels, and plasma display panels. Among these flat panel display devices, liquid crystal display panels are widely used because of their low power consumption and decreased size. The liquid crystal display panel displays image data corresponding to a video signal by controlling an amount of light passing through a liquid crystal layer.

[0004] The liquid crystal display panel device includes a common electrode and a plurality of pixel electrodes for applying an electric field to a liquid crystal layer, and a plurality of switch devices for switching a video signal supplied to each of the plurality of pixel electrodes. Generally, thin film transistors (TFT) are used as the switch devices. The liquid crystal layer controls an amount of light transmitted according to an intensity of the electric field applied between the pixel electrode and the common electrode.

[0005] A plurality of TFTs and a plurality of pixel electrodes are formed on a lower substrate. A common electrode is formed on a upper substrate, or the lower substrate in accordance with a method of applying an electric field to the liquid crystal layer. Accordingly, in the case of a liquid crystal display panel device of a horizontal electric field method, the common electrode is disposed on the lower substrate along with the TFT and the pixel electrode. In the case of a liquid crystal display panel device of a vertical electric field method, the common electrode is formed on the upper substrate. In addition, liquid crystal display panel devices for displaying a color picture have a plurality of color filters provided on the lower substrate.

[0006] To increase a brightness of a picture, a liquid crystal display panel, as shown in FIG. 1, has a pixel electrode 12 connected to a drain electrode 11 of a TFT 10, a scanning line 16 connected to a gate electrode 15 with an overlapping signal line 14 that is connected with a source electrode 13. Accordingly, a high brightness liquid crystal display panel uses an organic insulating film, thereby increasing an aperture ratio of the pixel electrode. The organic insulating film is formed by coating an organic insulating material on a substrate and curing the coated organic insulating material. However, gases produced by the organic insulating material contaminate a rear of the substrate.

[0007] FIGs. 2A to 2F are cross sectional views along A-A' of FIG. 1 showing a manufacturing process for making a high brightness liquid crystal display panel according to the conventional art.

[0008] In FIG. 2A, a gate electrode 15 is provided on a transparent substrate 18. Aluminum(Al) or copper(Cu) are deposited on the substrate 18 by a sputtering process

to form a metal thin film. Then, the metal thin film is patterned by a photolithographic process, including a wet method, to form the gate electrode 15.

[0009] In FIG. 2B, a gate insulating film 19, an active layer pattern 21, and an ohmic contact layer pattern 23 are sequentially deposited on the substrate 18 to cover the gate electrode 15. An insulating material, such as silicon oxide or silicon nitride, is deposited on an entire surface of the substrate 18 including the gate electrode 15 by a chemical vapor deposition (CVD) process to form the gate insulating film 19. Subsequently, an undoped active layer of polycrystalline silicon or amorphous silicon, and an ohmic contact layer of polycrystalline silicon or amorphous silicon doped with an n-type or p-type impurity at a high concentration, are continuously deposited on the gate insulating film 19 by a CVD process. The active layer and the ohmic contact layer is patterned by a photolithographic process that includes anisotropic etching, to remain only at a portion corresponding to the gate electrode 19. Thus, an active layer pattern 21, and an ohmic contact layer pattern 23 are prepared.

[0010] In FIG. 2C, drain and source electrodes 11 and 13 are formed on a surface and side portions of and the ohmic contact layer pattern 23, and on a side portion of the active layer pattern 21. Molybdenum (Mo) or a molybdenum alloy such as MoW, MoTa or MoNb, is deposited on the ohmic contact layer 23 and the exposed gate insulating film 19 by CVD or sputtering processes. The deposited metal layer or metal alloy layer is patterned by a photolithographic process, thereby forming the drain electrode 11 and the source electrode 13. During patterning of the drain electrode 11 and the source electrode 13, a portion of the ohmic contact layer pattern 23

corresponding to an upper portion of the gate electrode 15 is removed, thereby exposing a portion of the active layer pattern 21 and forming a channel located between the drain electrode 11 and the source electrode 13.

[0011] In FIG. 2D, a protective layer 25 is prepared on an entire surface of the substrate 18 corresponding to the drain electrode 11 and the source electrode 13. Organic insulating material, having small dielectric constant, such as acrylic organic compound, Teflon7, benzocyclobutene (BCB), Cytop7 or perfluorocyclobutane(PFCB), is coated on the substrate 18 by a spin-on-glass method, thereby flattening an upper surface of the protective layer 25. However, the organic insulating material can unnecessarily adhere to the rear of the substrate 18 during processing. Accordingly, a rear of the substrate 18 is contaminated with an impurity 25A of organic insulating material when the protective layer 25 of organic insulating material is formed.

[0012] In FIG. 2E, the protective layer is patterned by a photolithographic process to form a contact hole 17a, thereby exposing a portion of the drain electrode 11.

[0013] In FIG. 2F, a transparent electrode material, such as indium-tin-oxide (ITO), indium-zinc-oxide (IZO) or indium-tin-zinc-oxide(ITZO), is deposited on an entire surface of the protective layer 25 where the contact hole 17a is formed. The transparent electrode material is patterned by a CVD process to form a pixel electrode 12.

[0014] In FIG. 3, a lower substrate 18 on which the TFT and the pixel electrode are formed, is bonded to an upper substrate 28 on which a common electrode (not shown)

and/or color filters (not shown) are prepared. Before bonding the lower substrate 18 to the upper substrate 28, an alignment film (not shown) is printed on the lower substrate 18 for the injection of liquid crystal molecules, and then the printed alignment film (not shown) is rubbed. A sealant 27 is formed to provide cell gap at an edge portion of a surface of the lower substrate 18 where the alignment film (not shown) is prepared. Accordingly, another alignment film (not shown) is formed to cover the common electrode (not shown) on the upper substrate 28, and is rubbed. Thus, the lower substrate 18 is bonded to the upper substrate 28, thereby creating a space between the lower and upper substrates 18 and 28. Furthermore, the alignment film (not shown) formed on the upper substrate 28 faces the alignment film (not shown) on the lower substrate 18.

[0015] In FIG. 4, the bonded surface of the upper substrate 28 and rear of the lower substrate 18 are etched to reduce a thickness of the liquid crystal display panel. However, the rear of the lower substrate 18 and the surface of the upper substrate 28, is not uniformly etched due to contamination from the organic insulating material. Accordingly, a stain 25B is created by projection at a place where the contamination resides, thereby distorting image data. To prevent creation of the stain 25B, a grinding process is used on the surface of the upper substrate 28 and the rear of the lower substrate 18. However, the grinding process does not result in a liquid crystal display panel having a uniform thickness. Moreover, the grinding process is performed manually, thereby decreasing an efficiency of the fabrication process.

SUMMARY OF THE INVENTION

[0016] Accordingly, the present invention is directed to a method of fabricating a liquid crystal display panel that substantially obviates one or more of the problems due to limitations and disadvantages of the related art.

[0017] An object of the present invention is to provide a fabricating method of a liquid crystal display panel with high brightness and a reduced profile.

[0018] Another object of the present invention is to provide a fabricating method of a liquid crystal display panel having a uniform thickness.

[0019] Another object of the present invention is to provide a fabricating method of a liquid crystal display panel with an improved efficiency.

[0020] Additional features and advantages of the invention will be set forth in the description which follows, and in part will be apparent from the description, or may be learned by practice of the invention. The objectives and other advantages of the invention will be realized and attained by the structure particularly pointed out in the written description and claims hereof as well as the appended drawings.

[0021] To achieve these and other advantages and in accordance with the purpose of the invention, as embodied and broadly described, a method of fabricating a liquid crystal display panel includes preparing an upper substrate and a lower substrate, bonding the upper substrate to the lower substrate, cleaning exposed surfaces of the bonded upper and lower substrates, and eliminating the exposed surfaces of the bonded upper and lower substrates.

[0022] In another aspect, a method of fabricating a liquid crystal display panel includes bonding an upper substrate to a lower substrate, cleaning exposed surfaces of the bonded upper and lower substrates, and removing the exposed surfaces of the bonded upper and lower substrates.

[0023] In another aspect, a method of fabricating a liquid crystal display panel includes forming a gate electrode on a lower substrate, forming a gate insulating film on the lower substrate to cover the gate electrode, forming an active layer on the gate insulating film, and forming a source electrode and a drain electrode on the active layer, bonding an upper substrate to the lower substrate, cleaning exposed surfaces of the bonded upper and lower substrates, and removing the exposed surfaces of the bonded upper and lower substrates.

[0024] It is to be understood that both the foregoing general description and the following detailed description are exemplary and explanatory and are intended to provide further explanation of the invention as claimed.

BRIEF DESCRIPTION OF THE DRAWINGS

[0025] The accompanying drawings, which are included to provide a further understanding of the invention and are incorporated in and constitute a part of this specification, illustrate embodiments of the invention and together with the description serve to explain the principles of the invention. In the drawings:

[0026] FIG. 1 is a plan view showing a liquid crystal display panel according to the conventional art;

[0027] FIGs. 2A to 2F are cross sectional views showing a fabricating method of the liquid crystal display panel along I-I' of FIG. 1;

[0028] FIG. 3 is a cross sectional view showing a section of bonded lower and upper substrates according to the conventional art;

[0029] FIG. 4 is a cross sectional view showing an etching process of bonded lower and upper substrates according to the conventional art;

[0030] FIGs. 5A to 5I are cross sectional views showing an exemplary fabricating method of a liquid crystal display panel according to the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0031] FIGs. 5A to 5I are cross sectional views showing an exemplary fabricating method of a liquid crystal display panel according to the present invention.

[0032] In FIG. 5A, a gate electrode 15 may be formed on a lower substrate 18. Aluminum (Al) or copper (Cu), may be deposited on the substrate 18 by a sputtering process, for example, thereby forming a metal thin film on the substrate 18. Then, the metal thin film may be patterned by a photolithographic process including a wet etching method, for example, thereby forming a gate electrode 15.

[0033] In FIG. 5B, a gate insulating film 19, an active layer pattern 21, and an ohmic contact layer pattern 23 may be sequentially deposited on the substrate 15 to cover the gate electrode 15. Insulation material such as silicon oxide or silicon nitride, for example, may be deposited by a CVD process, for example, on an entire surface of the

substrate 18 having the gate electrode 15, thereby forming the gate insulating film 19. Subsequently, an active layer of undoped amorphous silicon or polycrystalline silicon, for example, and an ohmic contact layer of amorphous silicon or polycrystalline silicon doped with an n-type or p-type impurity at a high concentration, for example, may be deposited on the gate insulating film 19 by a CVD process, for example. The deposited active and ohmic contact layers are patterned by a photolithographic process including an anisotropic etching process, thereby forming the active layer pattern 21 and the ohmic contact layer pattern 23.

[0034] In FIG. 5C, drain and source electrodes 11 and 13 may be formed on surface and side portions of the ohmic contact layer pattern 23, and on a side portion of the active layer pattern 21. Molybdenum (Mo) or a molybdenum alloy such as MoW, MoTa or MoNb, for example, may be deposited on the ohmic contact layer 23 and an exposed portion of the gate insulating film 19 by CVD or sputtering processes. The deposited metal layer or metal alloy layer may be patterned by a photolithographic process, thereby forming the drain and source electrodes 11 and 13. In addition, when the drain and source electrodes 11 and 13 are patterned, a portion of the ohmic contact layer pattern 23 corresponding to an upper portion of the gate electrode 19 may be removed, thereby exposing a channel region of the active layer pattern 21 between the drain electrode 11 and the source electrode 13.

[0035] In FIG. 5D, a protective layer(25) may be prepared on an entire surface of the substrate 18 on which the drain electrode 11 and the source electrode 13 are formed. An organic insulating material having small dielectric constant, such as an acrylic

organic compound of Teflon7, benzocyclobutene (BCB), Cytop7 or perfluorocyclobutane (PFCB), for example, may be made coated on the substrate 18 by a spin-on-glass method, for example, to flatten an upper surface of the protective layer 25. However, the organic insulating material can unnecessarily adhere to a rear of the substrate 18. Accordingly, the rear of the substrate 18 is contaminated with an impurity 25A of organic insulating material w`hen the protective layer 25 is formed.

[0036] In FIG. 5E, the protective layer 25 may be patterned by a photolithographic process, thereby forming a contact hole 17a exposing a portion of the drain electrode 11. A transparent electrode material, such as ITO, IZO or ITZO, for example, may be deposited on an entire surface of the protective layer 25 where the contact hole 17a is formed.

[0037] In FIG. 5F, the transparent electrode material may be patterned by a CVD process, thereby forming a pixel electrode 12 on the protective layer 25.

[0038] In FIG. 5G, an alignment film (not shown) for aligning liquid crystal cells may be printed on an upper portions of the protective layer 25 and the pixel electrode 12 formed on the lower substrate 18, and then rubbed. A sealant 27 may be formed to provide a cell gap on an edge of a surface of the lower substrate 18 where the alignment film is prepared. While the lower substrate 18 is fabricated, an upper substrate 28 is also prepared. A common electrode (not shown) and/or color filters (not shown) may be formed on the upper substrate 28. Upon the preparation of the common electrode (not shown) and/or the color filers (not shown), the alignment film (not shown) may be

printed, for example, on the upper substrate 28. The alignment film on the upper substrate 28 is also rubbed. Thus, the lower substrate 18 is bonded to the upper substrate 28, thereby creating a space therebetween. Accordingly, the alignment film on the upper substrate 28 faces the alignment film on the lower substrate 18.

[0039] In FIG. 5H, the bonded surface of the upper substrate 28 and rear of the lower substrate 18 may be cleaned, thereby removing an impurity 25A of the organic insulating material. Moreover, the bonded surface of the upper substrate 28 and the rear of the lower substrate 18 may be dry-etched to have the impurity 25A completely removed.

[0040] In FIG. 5I, the lower and upper substrates 18 and 28 may be wet-etched while being dipped in an etching liquid, for example, to reduce a thickness of the lower and upper substrates 18 and 28. Accordingly, a thickness of the liquid crystal display panel from the bonded surface of the upper substrate 28 to the bonded rear of the lower substrate 18 is reduced by the wet etching. In addition, the impurity 25A may be removed in advance of the wet-etching so that the rear of the lower substrate 18 and the surface of the upper substrate 28, thereby preventing formation of a stain.

[0041] It will be apparent to those skilled in the art that various modifications and variations can be made in the method of fabricating a liquid crystal display panel of the present invention without departing from the spirit or scope of the invention. Thus, it is intended that the present invention cover the modifications and variations of this invention provided they come within the scope of the appended claims and their equivalents.